REMARKS

Applicants provide the present Amendment to respond to the Official Action mailed December 22, 2004. Applicants appreciate the indication of allowance of Claims 9-16 and of allowable subject matter in Claims 3-6, 8 and 18-20. Applicants have not amended the claims as Applicants submit that the claims are patentable over the cited reference.

Claim Objections

Claim 19 is objected to as the Official Action states that there is no antecedent basis for "the isolation layer" in Claim 19. Applicants respectfully submit that Claim 17 recites "an isolation layer" and, therefore, proper antecedent basis for the term "the isolation layer" is provided. Accordingly, Applicants request that the objection to Claim 19 be withdrawn.

The Claims Are Not Anticipated

Claims 1, 2, 7 and 17 stand rejected under 35 U.S.C. § 102(b) as anticipated by EP 1091417A1 to Skotnicki *et al.* Applicants note that the EP application is published in a foreign language and, therefore, will make their remarks with reference to U.S. Patent No. 6,495,403 to Skotnicki *et al.* (hereinafter "Skotnicki") which appears to claim priority from the same French application as the EP application and appears to have the same drawings as the EP application. Applicants request that the Examiner identify any differences between the EP application and Skotnicki if such differences are germane to the arguments Applicants make herein with reference to Skotnicki. Applicants will address each of the rejected independent claims below.

With regard to Claim 1, Applicants submit that the U.S. Skotnicki patent does not appear to disclose each of the recitations of Claim 1. In particular, Claim 1 recites:

> 1. (Original) A double gate MOS transistor comprising:
> a substrate active region defined in a semiconductor substrate;
> a transistor active region located over the substrate active region and overlapped with the substrate active region;
> **at least one semiconductor pillar penetrating the transistor active region and being in contact with the substrate active region**, the at least one semiconductor pillar supporting the transistor active region so that the transistor active region is spaced apart from the substrate active region;

at least one bottom gate electrode substantially filling a space between the transistor active region and the substrate active region, the at least one bottom gate electrode being insulated from the substrate active region, the transistor active region and the semiconductor pillar; and

at least one top gate electrode crossing over the transistor active region, and having at least one end that is in contact with a sidewall of the at least one bottom gate electrode, the at least one top gate electrode overlapping with the bottom gate electrode and being insulated from the transistor active region.

Applicants submit that at least the highlighted portion of Claim 1 is not disclosed or suggested by Skotnicki.

In particular, the Official Action cites to item 5b of Skotnicki as disclosing the semiconductor pillar recited in Claim 1. Official Action, p. 3. However, the portion 5b is not in contact with the substrate active region 2, but is, in fact, in contact with the "peripheral insulating region 3." *See* Skotnicki, col. 5, lines 11-19 and Figs. 1A-1E. As such, Skotnicki does not appear to disclose or suggest each of the recitations of Claim 1. Accordingly, Applicants submit that Claim 1 is not anticipated by Skotnicki. Applicants submit that the dependent claims are patentable at least as depending from a patentable base claim.

With regard to Claim 17, Applicants also submit that each of the recitations of Claim 17 are not disclosed or suggested by Skotnicki. In particular, Claim 17 recites:

17. (Original) A double gate MOS transistor comprising:

an isolation layer formed at a portion of a semiconductor substrate to define a substrate active region;

a transistor active region disposed over the substrate active region and overlapped with the substrate active region;

a first semiconductor pillar and a second semiconductor pillar disposed at both sides of the transistor active region respectively, **the first and second semiconductor pillars contacting the substrate active region**;

a bottom gate electrode substantially filling a space between the transistor active region and the substrate active region, the bottom gate electrode being insulated from the substrate active region, the transistor active region, the first semiconductor pillar and the second semiconductor pillar; and

first and second parallel top gate electrodes crossing over the transistor active region, each of the first and second top gate electrodes having both ends that are in contact with sidewalls of the bottom gate electrode, and the first and second top gate electrodes being located between the first and second semiconductor pillars to overlap with the bottom gate electrode.

Applicants submit that at least the highlighted portion of Claim 17 is not disclosed or suggested by Skotnicki. *See* Official Action, p. 5; Skotnicki, col. 5, lines 11-19 and Figs. 1A-1E.

As discussed above with reference to Claim 1, the cited regions 5b of Skotnicki are not provided in contact with the substrate active region 2 but are provided on insulating regions 3. As such, Skotnicki does not appear to disclose or suggest each of the recitations of Claim 17. Accordingly, Applicants submit that Claim 17 is not anticipated by Skotnicki.

Conclusion

In light of the above discussion, Applicants submit that the present application is in condition for allowance, which is respectfully requested.

Respectfully submitted,

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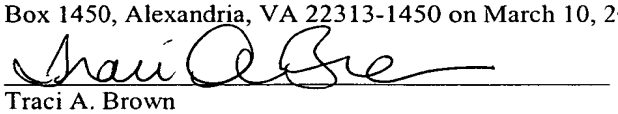

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